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Applicants: Bruce R. Scharf *et al.*

Serial No.: 10/000,232

Filed: November 30, 2001

For: DIFFRACTION
COMPENSATION USING A
PATTERNED REFLECTOR

Docket No.: 5557.P005

Examiner: James Phan

Art Unit: 2872

DECLARATION OF BRUCE R. SCHARF AND TROY DAIBER
37 C.F.R. § 1.131

We, Bruce R. Scharf and Troy Daiber, hereby declare as follows:

1. We are joint inventors of the invention described and claimed in the above-captioned patent application.

2. Upon information and belief, the Examiner has rejected all claims in the above-captioned application as anticipated under 35 U.S.C. § 102(e) by U.S. Patent No. 6,506,620 to Scharf *et al.*, which has a filing date of November 27, 2000 (hereinafter the "Reference Date").

3. Prior to the Reference Date and until at least the filing date of the above-captioned application, both of us were employees of Microscan Systems, Inc. (hereinafter "Microscan"), the assignee of the entire right, title and interest in the above-captioned application.

4. Prior to the Reference Date, we conceived the invention described and claimed in the above-captioned application. Conception is illustrated by Exhibits A1-A5,

all of which have had the dates redacted but all of which were produced prior to the Reference Date. Exhibits A1-A5 are explained as follows:

- (a) Exhibit A1 is an invention disclosure form authored by Mr. Scharf. The invention disclosure form discusses diffraction compensation on MOEMS devices using diffractive elements.
- (b) Exhibit A2 is a page from Mr. Scharf's laboratory notebook describing using a reflective element for diffraction compensation in the MOEMS device proposed in Exhibit A1.
- (c) Exhibit A3 is a preliminary design of a prototype MOEMS scanning mirror including a Fresnel pattern thereon, thus incorporating the concepts described in Exhibits A1 and A2.
- (d) Exhibit A4 is a production-ready layout produced by Mr. Andrew Zosel of Microscan that was designed to be used by a MEMS manufacturer to build a chip including prototypes of devices in the layout. The layout incorporates the concepts described in Exhibits A1 and A2 in a patterned reflector (noted on the exhibit) that can be rotated out of plane using a pair of comb drives (also noted on the exhibit).
- (e) Exhibit A5 is a photograph of a chip including the prototype MOEMS devices manufactured using Exhibit A4. The chip shown in Exhibit A5 was received by Microscan at or near the end of October 2001 (*see* Exhibits B1-B18).

5. After conception of the invention described and claimed in the above-captioned patent application, Microscan became a partner in a consortium of companies

seeking to develop micro-electro-mechanical systems (MEMS) and micro-opto-electro-mechanical systems (MOEMS).

- (a) The consortium agreement was designed in part to allow consortium partners to examine the feasibility of manufacturing MEMS or MOEMS applications useful for their particular market or industry.
- (b) The consortium included development partners who developed prototype MEMS or MOEMS applications and a manufacturing partner to manufacture the prototypes designed by the development partners.
- (c) Microscan and Xerox Corporation ("Xerox") were two of the development partners in the consortium, and Standard MEMS, Inc. (hereinafter "Standard MEMS") was one of the manufacturing partners.
- (d) Mr. Joel Kubby of Xerox was the person in charge of coordinating among the partners during the life of the consortium. Mr. Scharf was Microscan's representative in matters relating to the consortium.
- (e) Development was split into four phases or "mask sets": Mask Set 0, Mask Set 1, Mask Set 2, and Mask Set 3. Each mask set was intended to include MEMS or MOEMS devices more complex than those of the previous mask set, based on information learned during manufacture of devices from previous mask sets.
- (f) Each Mask Set included a certain amount of reserved space for each development partner. All development partners would contribute their prototype designs, and the contributions of all development partners were assembled into a single Mask Set.

- (g) To determine the feasibility of building the present invention, Microscan submitted the layout of Exhibit A4, which included the present invention, to the consortium to be incorporated into Mask Set 1.
- (h) Mask Set 1 was manufactured by Standard MEMS.

6. Beginning prior to the Reference Date, we exercised diligence in obtaining an actual reduction to practice of the invention claimed in the above-captioned patent application, as illustrated by Exhibits B1 to B18 attached hereto. Exhibits B1 to B18 are explained as follows:

- (a) Exhibit B1 (February 3, 2000) is an e-mail from Mr. Andrew Zosel of Microscan to the other partners transmitting electronic files containing, among other things, the data for the layout shown in Exhibit A4.
- (b) Exhibit B2 (March 7, 2000) is an e-mail from Mr. Kubby to partners forwarding a request from Dr. Raji Mali of Standard MEMS for any corrections to Mask Set 1.
- (c) Exhibit B3 (March 9, 2000) is an e-mail from Mr. Zosel to Mr. Kubby and Dr. Mali, indicating that corrections to Mask Set 1 had been made.
- (d) Exhibit B4 (April 5, 2000) is a string of e-mails between Mr. Zosel and Mr. Kubby, indicating that Mr. Zosel had reviewed check plots of Mask Set 1.
- (e) Exhibit B5 (May 2, 2000) is an e-mail from Mr. Kubby to the partners indicating that the fabrication schedule had slipped by 11 months, with fabrication expected to start May 1, 2000, and end January 26, 2001.
- (f) Exhibit B6 (June 26, 2000) is an e-mail from Mr. Kubby to the partners, indicating that the schedule had slipped further by one month.

- (g) Exhibit B7 (October 26, 2000) is an e-mail from Mr. Kubby to the partners forwarding an e-mail from Donna Zaharek at Standard MEMS indicating that Mask Set 1 wafers were still being processed.
- (h) Exhibit B8 (December 21, 2000) is an e-mail from Mr. Kubby to the partners forwarding a question from Mr. de Lanerolle of Standard MEMS and asking if it affects any of the partners.
- (i) Exhibit B9 (January 18, 2001) is an e-mail from Mr. Kubby to the partners regarding the processing steps followed for Mask Set 1 and upcoming discussions for Mask Set 2.
- (j) Exhibit B10 (March 12, 2001) is an e-mail from Mr. Kubby to the partners forwarding an e-mail from Mr. de Lanerolle of Standard MEMS indicating that completion of Mask Set 1 was now expected at the end of March 2001.
- (k) Exhibit B11 (March 30, 2001) is an e-mail from Mr. Peter Gulvin of Xerox to Mr. Kubby and to Mr. de Lanerolle of Standard MEMS identifying potential causes of, and proposing solutions to, Mask Set 1 production problems still plaguing Standard MEMS.
- (l) Exhibit B12 (April 4, 2001) is an e-mail exchange between Mr. Kubby and Mr. Delvecchio of Standard MEMS proposing solutions for further Mask Set 1 production problems plaguing Standard MEMS.
- (m) Exhibit B13 (April 19, 2001) is an e-mail sent by Mr. Kubby to Mr. Scharf indicating frustration with the continued Mask Set 1 production problems at Standard MEMS and suggesting that the partners arrange an alternate supplier to replace Standard MEMS.

- (n) Exhibit B14 (June 17, 2001) is an e-mail from Mr. Kubby to the partners regarding a meeting on August 2-3, 2001, to coordinate testing of Mask Set 1 devices when finished.
- (o) Exhibit B15 (August 3, 2001) is a schedule produced at the coordination meeting. The schedule indicates that, at the time, Mask Set 1 was scheduled to be finished on September 30, 2001, and that Mask Set 1 post-processing and testing would take place between September 30 and October 15, 2001.
- (p) Exhibit B16 (August 12, 2001) is an e-mail from Mr. Kubby to the partners forwarding a question from Standard MEMS regarding back-side gold metallization.
- (q) Exhibit B17 (September 7, 2001) is an e-mail from Mr. Kubby to the partners indicating that there were problems in releasing components from a preliminary batch of wafer received from Standard MEMS.
- (r) Exhibit B18 (September 28, 2001) is an e-mail from Mr. Kubby to the partners indicating that delivery of corrected wafers from Standard MEMS were expected about October 15, 2001.

7. At or near the end of October 2001, Microscan received completed Mask Set 1 chips from Standard MEMS, one of which included the prototype devices that had been submitted in the layout of Exhibit A4. A photograph of this chip is shown in Exhibit A5.

8. Having received the prototypes and confirmed the feasibility of manufacturing the invention, Microscan directed its patent attorney, Mr. Todd Becker, to file a patent application describing and claiming the invention.


9. The patent application was filed on November 30, 2001 and became the above-captioned patent application.

10. All statements made herein based on our own knowledge are true, and any statements made upon information and belief are believed to be true. We understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the application or any patent issuing thereon.


* * * *

Respectfully submitted,

Date: 12/2/2005


Bruce R. Scharf

Date: 12/2/2005


Troy Daiber

ATP



ATP Proposal Invention Disclosure

TITLE: Aperture Diffraction Compensation using Fresnel Lens		I.D. NUMBER: MS-1
FUNCTION: Reduce diffraction of focused laser		
COMPANY: Microscan Systems Inc		DATE: [REDACTED]
INVENTOR(S): Bruce Scharf		TELEPHONE: (425) 226-5700
STATUS(MODEL, PROTOTYPE OR EXPERIMENT BEEN BUILT, MADE, RUN OR TESTED?): Model	FILE <input type="checkbox"/> YES PATENT <input checked="" type="checkbox"/> NO	DATE OF INVENTION: [REDACTED]
- INVENTION DESCRIPTION -		
<p>Laser diodes used for optical scanning employ beam forming optics to create a optical energy distribution suitable for the application. In bar code readers, for example, a small spot (<100 microns at $1/e^2$) is required for scanning high density labels. Edge emitting laser diodes have a highly elliptical, astigmatic beam that requires lenses and apertures for successful beam forming. Current methods place the beam forming elements outside of the diode laser package. The result is that the laser spot is large by the time it reaches the optics. This means that the optics must focus the beam back down to a small spot and hence the depth of field is small. Furthermore, the aperture can cause diffraction effects which also limits system performance.</p> <p>The proposed invention helps solve the beam forming problems. First, by capturing the laser emission close to the diode, the spot size can be minimized over a larger depth of field. Second, the diffraction can be reduced by employing a diffractive (fresnel) rather than refractive lens. Furthermore, in Micro-Optical Mechanical Systems, the lens and aperture can be combined by varying the thickness of the lens in the radial direction, and hence the transmission. A gaussian profile can be used to further improve the performance of the beam forming system. These methods would be applicable even if a non-astigmatic surface emitting laser is employed.</p>		
ADVANTAGES		DISADVANTAGES
<ul style="list-style-type: none"> • Improved beam quality with fewer elements • In MOEMS, more efficient due to proximity to emission source • • • • • • 		<ul style="list-style-type: none"> • More complex to fabricate • • • • • • •

Ext Briefing with Jon Blanchard
C: Mydocs 336 Mbytes
→

UV Ink
Illuminate with 366 nm
vents @ 440 nm

IR probe
illuminate @ 670 nm
emit @ 680 nm

B. Blanchard

Modify MOEMS device to include Fresnel
as a REFLECTIVE device!



UV Ink

called Ron Stevens @ 2:30 pm
619-655-6989

vision system filter
under Emission Distribution (hard to pinpoint)
that use 2 690-700 nm emission
Hologen 650 cutoff filter illumination
700 nm cut-off low pass filter
bandpass filter on vision probe

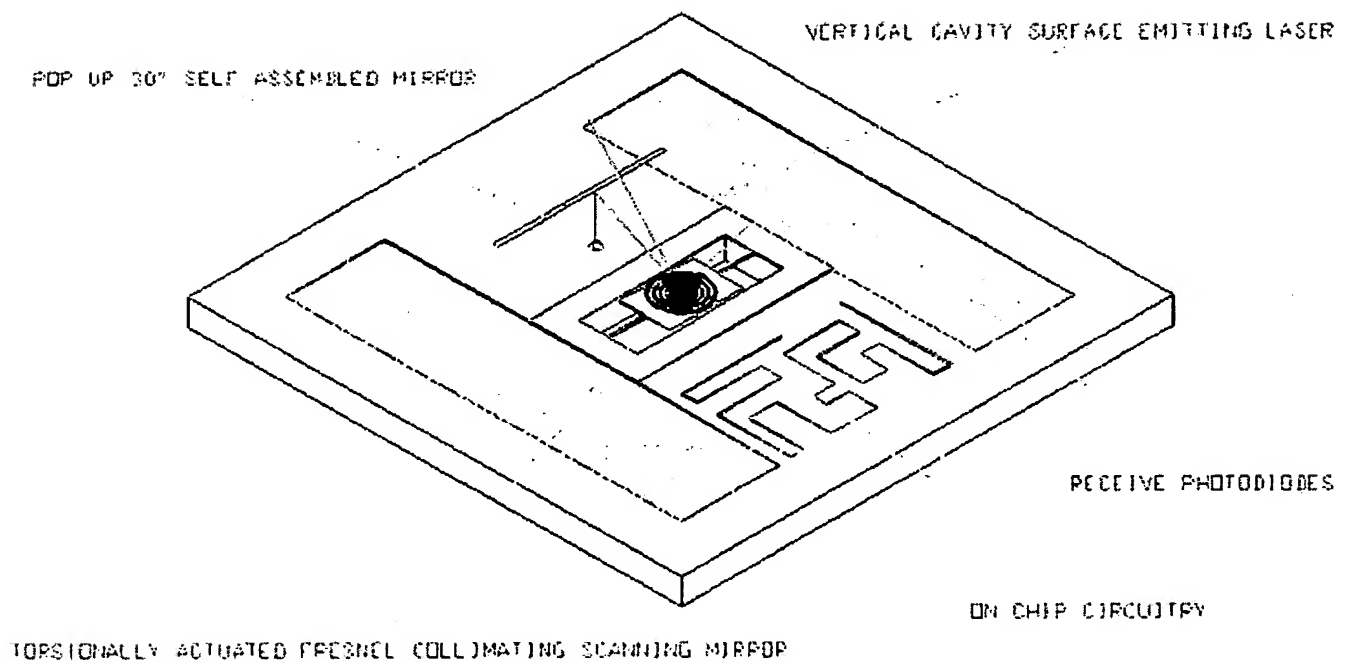
OCLE
Jennie

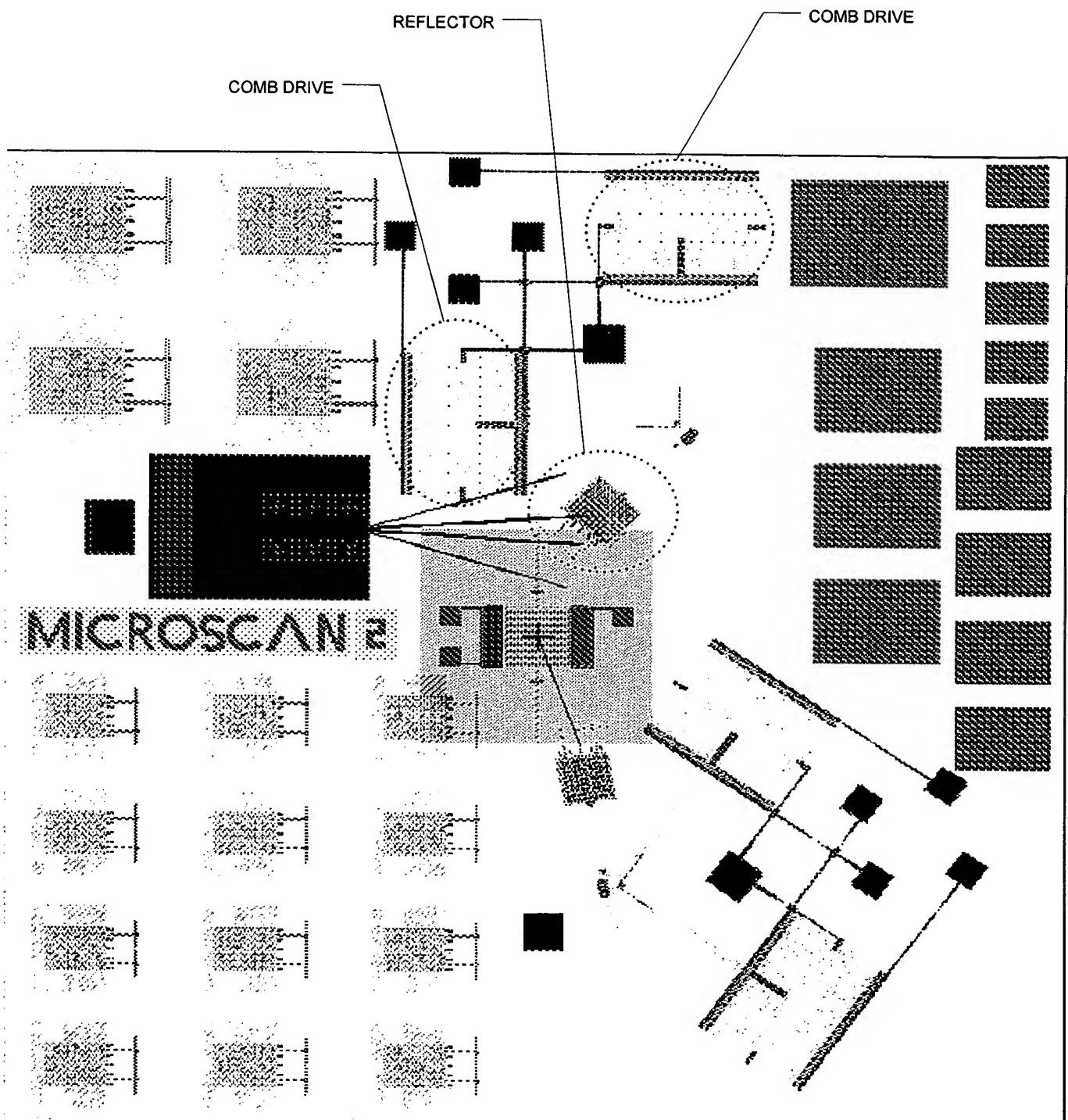
707-525-7012

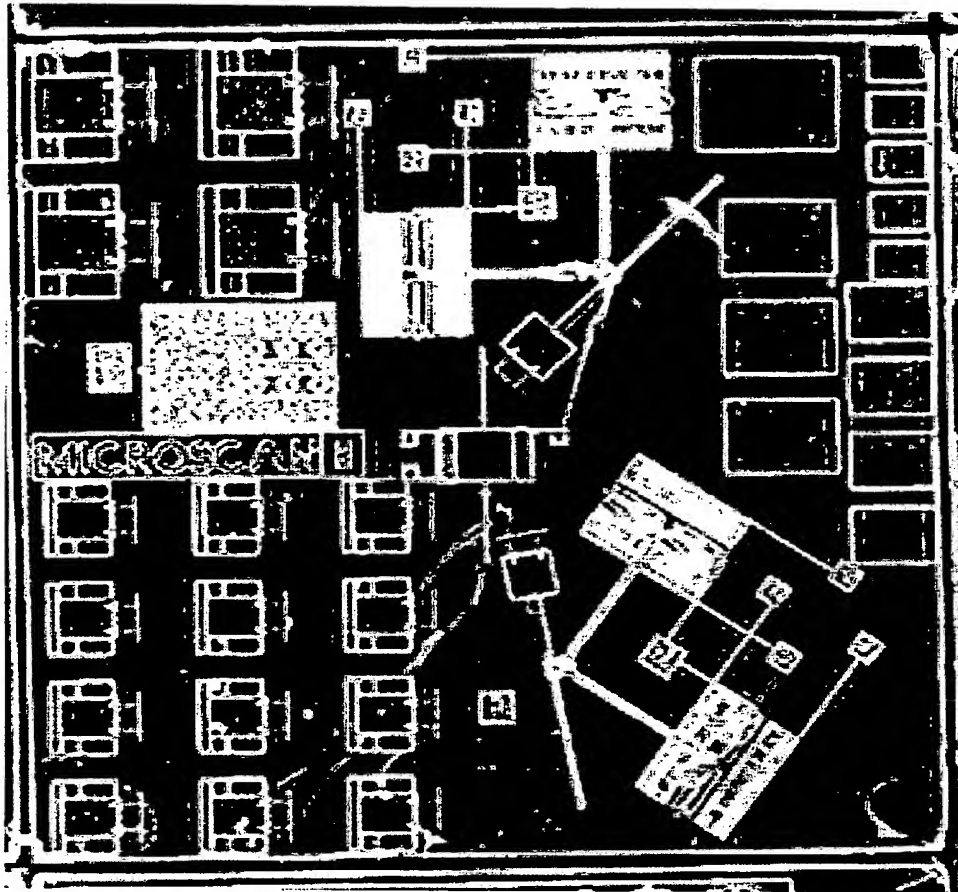
Requested sample of 700 nm ± 20 nm
filter. She will get back to me.

sendng price of filter overnight 1/6/99

MICROSCAN HIGH SPEED MOEMS SCANNER







*U.S. Patent Application Serial No. 10/000,232
Declaration of Bruce R. Scharf and Troy Daiber
Exhibit A5*



From: Andy zosel
To: "ahusain@omminc.com"@Microscan.GWIA; "art@memcad...."
Date: Thu, Feb 3, 2000 10:32 AM
Subject: Re: ATP Mask Set 1 Submission Meeting, Monday, 2/7, 3-4 PM (EST) — Microscan's Submission

All,

I have attached ten .gds files zipped together. If you have the opportunity to review these files and provide feedback please do so. As long as there are no show stopping mistakes this will be Microscan's design contribution to Mask Set 1.

Thank You,

Andrew Zosel
Opto-Mech Engr. Dpt. Mngr.
Microscan Systems
1201 SW 7th St
Renton, WA 98055
(425) 226-5700
Fax (425) 254-9295

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Alex Tran <ATran@crt.xerox.com>, Andy zosel <azose...
Date: Tue, Mar 7, 2000 3:12 PM
Subject: FW: Mask set 1 layout data - more corrections

All, FYI. Could each partner with designs in Mask Set 1 please try to respond with your fix by the end of the day on Thursday, March 9th? If you have any questions please ask Raji via e-mail with the group copied in so that others can benefit from the discussion. Thanks for your input!

Regards,

Joel

—Original Message—

From: Raji.Mali@smc.com [mailto:Raji.Mali@smc.com]
Sent: Tuesday, March 07, 2000 5:27 PM
To: jkubby@crt.xerox.com
Cc: 'Alex Tung Tran'; 'Andy Zosel'; Lin, Chuang-Chia; Sun, Decai <sun@parc.xerox.com>; Chang, Jets; 'Jingkuang Chen'; 'Li Fan'; Rosa, Michel <mrosa@parc.xerox.com>; 'Vlad'; Nena.Golubovic@smc.com; Steve.DelVecchio@smc.com; Tom.Pumo@smc.com
Subject: Mask set 1 layout data - more corrections

All,

I have been working with some of you individually to fix some problems in the data. I now find a couple of things which could be potentially major problems, so please read on.

1. Substrate_contact layer

On the Substrate_Contact layer, designers were supposed to use only 4 um geometries so that the 2.5 um layer poly would planarize the surface. I find, however, some very large geometries on this layer. (e.g. MIC1007, MIC1008). Its possible other files have it also. This is a problem because there will be local non-planar regions and it could get messy during subsequent processing. If this was done intentionally, we can discuss what to do. If it was an oversight, it should be fixed. A second problem I found on this layer was that even with 4x4 um geometries, checkerboard patterns have been used. (e.g. XER1003, XER1004). We are not sure what will happen at intersecting corners on such a geometry.

2. Objects outside die extents

There are some rotated cells outside die extents. (e.g. XER1003, XER1004). Could be a bug in the software? These files will have to be fixed.

3. Scaling

All OMM files are scaled on a different internal unit system. The template we use has 1 micron = 1000 internal units. Please stick with this and update files accordingly.

4. Scribe

Finally, we think we overlooked the planarization issue in defining the scribe. I'd like to update it using the SCS_Expose instead of Anchor_SCS so the topography is created closer to the end of the process. Another minor change: Top_Level instead of _Top_Level.

Attached are the new template files and Excel file. Even if there are no corrections in a particular file, please re-export it using the new template so that everyone is consistent. You will also have to do a new layer list because the scribe is changing. Thanks for your co-operation on this.

(See attached file: atp1_tp8_v2.tdb)(See attached file: atp1_tp7_v2.tdb)(See attached file: atp1_tp6_v2.tdb)(See attached file: Atp_1.xls)

I think its well worth the extra time to fix these issues now rather than cause delays of weeks or months in the process cycle. Please feel free to call me if you have any questions.

Thanks,
Raji

Dr. Raji Mali
Standard MEMS Inc.
(516) 592 1419
Raji.Mali@smc.com

From: Andy zosel
To: "jkubby@crt.xerox.com"@Microscan.GWIA; "Raji.Mali...
Date: Thu, Mar 9, 2000 3:19 PM
Subject: Microscan Cells Updated

Raji,

I have corrected/updated the Microscan cells.

The wide areas of Substrate_Contact layer were from a cell I had copied from PARC (laser_bonding_pads_recessed).

Let me know if you have any questions.

Andrew Zosel
Opto-Mech Engr. Dpt. Mngr.
Microscan Systems
1201 SW 7th St
Renton, WA 98055
(425) 226-5700
Fax (425) 254-9295

CC: "CLin@crt.xerox.com"@Microscan.GWIA; "JChang@crt....

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: "Andy zosel" <azosel@microscan.com>, "Kubby, Joe...
Date: Wed, Apr 5, 2000 1:30 PM
Subject: RE: FYI Mask Set 1 Checkplots

Thanks Andy. Keep me updated on what you find.

Joel

-----Original Message-----

From: Andy zosel [mailto:azosel@microscan.com]
Sent: Wednesday, April 05, 2000 4:32 PM
To: JKubby@crt.xerox.com
Cc: Opto-man@microscan.com; TDaiber@microscan.com
Subject: FYI Mask Set 1 Checkplots

Joel,

I recieved check plots for one of my dies.

I have reviewed them and they looked accurate to me.

The only errors were ones that were in my design and should not significantly impair performance.

I will let you know when I receive the remaining plots and have validated them.

Thanks

Andrew Zosel
Opto-Mech Engr. Dpt. Mngr.
Microscan Systems
1201 SW 7th St
Renton, WA 98055
(425) 226-5700
Fax (425) 254-9295

>>> "Kubby, Joel A" <JKubby@crt.xerox.com> 04/05 10:23 AM >>>
Thanks Andy. Let me know if you find any problems. I will try to set up a teleconference call after everyone has had a chance to look at their layouts.

Regards,

Joel

-----Original Message-----

From: Andy zosel [mailto:azosel@microscan.com]
Sent: Wednesday, April 05, 2000 12:44 PM
To: JKubby@crt.xerox.com
Subject: Re: RE: Mask Set 1 Checkplots

They just arrived!

*U.S. Patent Application Serial No. 10/000,232
Declaration of Bruce R. Scharf and Troy Daiber
Exhibit B4 (page 1 of 2)*

>>> "Kubby, Joel A" <JKubby@crt.xerox.com> 04/05 8:41 AM >>>
Thanks Andy. Let me know when you get them. Regards, Joel

-----Original Message-----

From: Andy zosel [mailto:azosel@microscan.com]
Sent: Wednesday, April 05, 2000 11:40 AM
To: JKubby@crt.xerox.com
Subject: Re: Mask Set 1 Checkplots

Nothing yet.

>>> "Kubby, Joel A" <JKubby@crt.xerox.com> 04/05 6:58 AM >>>
Andy and Li,

Could you let me know if you have received your mask set 1 checkplots? Mike Rosa has received one of his checkplots and one of someone else's checkplots. Peter Gulvin has not yet received any checkplots. Please let us know what you have received.

Thanks,

Joel

> Joel Kubby
> Marking Element Lab/Specialty Sensors
> Xerox Wilson Center for Research and Technology
> 800 Phillips Road, M/S W-114-38D
> Webster, New York 14580-9701
>
> Office: Building 114 Room 358
> phone: (716) 422-9609
> fax: (716) 265-5080
> EMail = JKubby@crt.xerox.com (Business)
> EMail = KB2TXM@aol.com (Personal)
>
>

CC: "Gulvin, Peter" <PGulvin@crt.xerox.com>

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Eric Peeters <peeters@parc.xerox.com>, Joel Kubby ...
Date: Tue, May 2, 2000 5:10 PM
Subject: FW: ATP MASK SET 1

<<MOEMS Manufacturing Y2K Schedule.rtf>>
All,

Please find attached a schedule for the Mask Set 1 fabrication run (below), and a copy of our 2000 schedule that we developed at our 1Q00 meeting (above). We are currently two months behind our intended start date for the Mask Set 1 fabrication run (5/1/00 instead of 3/06/00), and the new estimate for the fabrication run is 9 months (5/1/00 to 1/26/01) rather than the 6 months (3/06/00 to 9/01/00) in the original plans. In combination this will be an 11 month slip in schedule, and will seriously impact our ability to complete our plans for Mask Sets 2 and 3. I would like to set up a conference call to discuss what we would like to do in light of this schedule slip. I would propose that we set up the call for 4 PM (EDT) on Wednesday, May 3rd. If a representative from your company is unable to attend on this date, let me know and we can try to find an alternate date.

Regards,

Joel

-----Original Message-----

From: Nena.Golubovic@smc.com <mailto:Nena.Golubovic@smc.com>
[mailto:Nena.Golubovic@smc.com] <mailto:[mailto:Nena.Golubovic@smc.com]>
Sent: Monday, May 01, 2000 5:45 PM
To: JKubby@crt.xerox.com <mailto:JKubby@crt.xerox.com>
Subject: ATP MASK SET 1

<<Atp_ms1.mpp>>

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Alex Tran <ATran@crt.xerox.com>, Christopher Chua ...
Date: Tue, Jun 27, 2000 6:25 AM
Subject: FW: weekly update

All,

FYI on the Mask Set 1 status. We are currently at step 15 of the process (see below), which was originally scheduled to start on 5/26, putting us 1 month behind our original schedule.

Regards,

Joel

"F4 POLY DEP (590 deg., 2.5 um) recipe _____" 2d Fri 5/26/00
Tue 5/30/00

-----Original Message-----

From: Donna.Zaharek@smc.com <mailto:Donna.Zaharek@smc.com>
[mailto:Donna.Zaharek@smc.com] <mailto:[mailto:Donna.Zaharek@smc.com]>
Sent: Monday, June 26, 2000 5:42 PM
To: jkubby@crt.xerox.com <mailto:jkubby@crt.xerox.com>
Cc: njia@crt.xerox.com; <mailto:njia@crt.xerox.com>;
Nena.Golubovic@smc.com <mailto:Nena.Golubovic@smc.com>
Subject: weekly update

Hi.....hope your Monday is going well.
I'm afraid this past week has not been as productive as we would have liked.
ATP-01 lead lot, 25032 is still waiting for the 3um poly dep (step 15).
The tube has been aborting each time the pass is started. Engineering has
made some progress in identifying the cause(s) for the abort and hopefully,
the dep will take place soon.

-DZ

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Christopher Chua <chua@parc.xerox.com>, Eric Peete...
Date: Fri, Oct 6, 2000 1:29 PM
Subject: FW: Status of ATP Mask Set 1 wafers

All,

FYI on the Mask Set 1 status:

"--> send to MIT: TEOS DEP, DENSE, --> CORNELL FOR CMP"	15 days	Wed
7/19/00 Wed 8/9/00 32		

Regards,

Joel

-----Original Message-----

From: Donna Zaharek [mailto:DZaharek@smems.com]
Sent: Friday, October 06, 2000 1:35 PM
To: 'Kubby, Joel A'
Cc: Nena Golubovic; Nimal De Lanerolle
Subject: RE: Status of ATP Mask Set 1 wafers

Hi Joel,

The wafers are still out for CMP.....Nimal would have details about when we should expect them back but I haven't been able to get ahold of him today to ask him.....

-DZ

-----Original Message-----

From: Kubby, Joel A [mailto:JKubby@crt.xerox.com]
Sent: Friday, October 06, 2000 8:33 AM
To: 'Donna Zaharek'
Cc: 'Nena Golubovic'
Subject: Status of ATP Mask Set 1 wafers

Donna,

Could you give me an update on the ATP Mask Set 1 wafers?

Thanks,

Joel

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Christopher Chua <chua@parc.xerox.com>, Eric Peete...
Date: Thu, Dec 21, 2000 2:02 PM
Subject: FW: ATP process flow question

All,

Please see the attached note below from Nimal. If this issue impacts your design in mask set 1 could you let me know?

Thanks,

Joel

-----Original Message-----

From: Nimal De Lanerolle [mailto:NDeLanerolle@smems.com]
<mailto:[mailto:NDeLanerolle@smems.com]>
Sent: Wednesday, December 20, 2000 6:31 PM
To: 'joel.kubby@crt.xerox.com'
Cc: Tom Purno; Nimal De Lanerolle
Subject: ATP process flow question

Hey Joel

I have a question regarding the poly to fill the dimple and substrate contact holes. For the poly to function as a contact medium it should be conductive and therefore doped. The poly 0 that comes on top of this poly gets doped by the densification of the PSG1 layer. However, it is unlikely that the entire plug of the contact poly (5u +) deep will get doped by this method. This was a major issue on another project I was working on earlier. My question then is two fold

1. Is the initial poly dep of 2.5 (or 3u on the first run) is meant as a contact medium.
2. Was it the intention for this poly to be doped.

Regards
Nimal de Lanerolle

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Christopher Chua <chua@parc.xerox.com>, Eric Peete...
Date: Thu, Jan 18, 2001 3:03 PM
Subject: Mask Set 1 Process

<<Mask Set 1 Process.doc>>

All,

Please find attached a list of steps that were used for the Mask Set 1 process. We can use this document to discuss changes we would like to make for Mask Set 2 at the upcoming 1Q01 meeting.

Regards,

Joel

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: Christopher Chua <chua@parc.xerox.com>, Eric Peete...
Date: Mon, Mar 12, 2001 10:54 AM
Subject: Outlook for Mask Set 1 parts

All,

Below is an update on the outlook for the completion of the Mask Set 1 parts.

Regards,

Joel

-----Original Message-----

From: Nimal De Lanerolle [mailto:NDeLanerolle@smems.com]
<mailto:[mailto:NDeLanerolle@smems.com]>
Sent: Monday, March 12, 2001 12:57 PM
To: 'Kubby, Joel A'
Cc: Tom Pumo; Abdoul Seck; Dave Kharas; Flora Briganti; Ed Look; John Fijol
Subject: RE: CMOS/DMOS device layer doping

We had problems with the etch machine which went down hard for 1 week. But the affect on the lots was much more. So will not be able to deliver by March 15. Looking more like end of March.
Nimal

From: "Gulvin, Peter" <PGulvin@crt.xerox.com>
To: "Kubby, Joel A" <JKubby@crt.xerox.com>, "Nimal De...
Date: Fri, Mar 30, 2001 1:48 PM
Subject: RE: ATP MOEMS mask set 1 status

Nimal,

About this paragraph:

The problem of non planarized wafers will appear on all subsequent lots. Unless a solution is found there will be unpredictable delays. Trying to find a solution is what we are doing now. Here I would appreciate help from Peter Gulvin. One approach we decided not to pursue, was to push on through 012 as best as we can. This was overruled in-house because we decided that the poly1 left behind in the uncleared areas is going to adversely impact the functioning of some of the mechanical devices. If what Steve is attempting is not going to work, it will also not work at 013 (poly 2), and as I see it, the consortium should then jointly make a decision on the quality of the progress we want to make with the current mask set 1. At the quarterly meeting SMI did request a revision of mask set 1, not quoting the above issues, because they had not occurred at that time.

The problem of the CMP depression comes from two effects, as I understand it. The first is that the surface used for polishing is flexible enough that if it's not supported by intermittent structures, it sags and polishes away extra material in the open spaces. If it's okay to change the masks, then one solution would be to add posts in the centers of the wide open areas so that there will be no large uninterrupted areas to be attacked by the CMP.

The second cause is that we're depending on the reflow of extra planarization oxide from high areas to fill into the low areas, but in these open areas there aren't any adjacent high areas to provide the extra oxide. Posts would only help slightly, since they wouldn't occupy a high percentage of area. To solve this we would need to fill in much more of the open areas. That would take more time, but it shouldn't be too bad if it's necessary. There may be some areas that need to remain open to leave room for structures to move.

Since we're using timed CMP, not stopping on a poly layer, I would guess that the second cause would be the main reason for what we're seeing, so the posts might not cut it.

So should we start altering the SCS mask? I believe some of the optical designs that Jets made were some of the worst offenders, but if we're changing the mask anyway, it might be worth fixing some other chips that are having less serious problems.

Also, about the poly etch not filling the cavities... Are the trenches being pinched-off by build-up of poly at the upper edge? If that's the case, I think the only solution is to work on making the poly deposition more conformal. That was the same problem that they had in Mask Set 0, except it was PSG that they were having trouble getting into Poly trenches.

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: "Steve Delvecchio" <SDelvecc@smems.com>, "Kubby,..."
Date: Wed, Apr 4, 2001 9:09 AM
Subject: RE: ATP mask set I process

Thanks for the update Steve. This seems like a possible fix for clearing the resist. What is the outlook for receiving the bias masks?

It still seems like there is a problem with the polysilicon filling large trenches. JK has some questions on this in his note below. Any thoughts on this?

Thanks,

Joel

-----Original Message-----

From: Steve Delvecchio [mailto:SDelvecc@smems.com]
Sent: Wednesday, April 04, 2001 11:42 AM
To: 'Kubby, Joel A'; Nimal De Lanerolle
Cc: Tom Pumo; Glenn Fricano; Nimal De Lanerolle; Ken Chin; John Fijol; 'G. V. Blessing'; Chen, Jingkuang; Steve Delvecchio; 'Opto-man@microscan.com'; 'lifan@omminc.com'; Abdoul Seck
Subject: RE: ATP mask set I process

Hi Joel,

We have already put in motion double exposure masks that will protect the first exposure for all the clear field (positive resist) layers.

We actually ordered the same plates with a larger bias. This will be attempted on the 012 layer first before we commit to the rest of the masks.

A negative resist approach in the future will be recommended but may require a considerable development effort.

That's it...
Steve DelVecchio
Standard MEMs Inc.
35 Marcus Blvd.
Hauppauge, NY 11788
(631) 592-1404
(631) 434-7360 Fax
sdelvecchio@smems.com

-----Original Message-----

From: Kubby, Joel A [mailto:JKubby@crt.xerox.com]
Sent: Tuesday, April 03, 2001 12:09 PM
To: 'ndelanerolle@smems.com'
Cc: Tom Pumo; Glenn Fricano; Nimal De Lanerolle; Ken Chin; John Fijol; 'G. V. Blessing'; Chen, Jingkuang; 'Steve Delvecchio';

*U.S. Patent Application Serial No. 10/000,232
Declaration of Bruce R. Scharf and Troy Daiber
Exhibit B12 (page 1 of 3)*

Seck' 'Opto-man@microscan.com'; 'lifan@omminc.com'; 'Abdulaye
Subject: FW: ATP mask set I process

Nimal,

Please find JK Chen's feedback below. He has an idea for
removing the residual photoresist in the clear field masks, and some
questions regarding the lack of poly fill in the trenches. Could you let us
know what you think of his solution and provide feedback on his questions?

I would also like to determine if the planarization problem
you have found is only associated with the one cell that includes the
design rule violation. Would it be possible to generate a map of the
wafer topography using your non-contact profilometer? If so we may be able
to correlate the areas that did not planarize with the cell containing this
design rule violation. If we can make this correlation then we could
run the Mask Set 1 designs again with this cell removed. If we are not able to
make this correlation then the fix will be less straightforward. Let
me know,

Thanks,

Joel

——Original Message——

From: Chen, Jingkuang
Sent: Tuesday, April 03, 2001 11:47 AM
To: Kubby, Joel A
Subject: ATP mask set I process

<<mask.doc>>

Joel,

Attached is a drawing regarding removing the residual
photoresist in the field region. Please feel free to make any change or add
your comments.

As I explained yesterday, the procedures are:
1. Photolithography using the original mask
2. Dry etching to pattern POLY1 (After this step, some
residual POLY1 will remain in some field areas because of residual photoresist on
recessed holes)
3. Strip photoresist

3um beyond the
The residual
cavities." my
LPCVD
This means it will
deposition.
posts on their
filled the
in touch with
a cross section
of what the
after cleaving
they used for
what is used at
problem.

4. Photolithography using the auxiliary mask which extends
edgea of the POLY1 patterns. Intentionally OVER-EXPOSE.
photoresist will be cleared.
5. RIE to strip the residual POLY1 on the field region.
6. Strip photoresist.

Regarding the second problem: "poly did not fill the large
comments are:
From my own experiences and what I learned from literature,
polysilicon has very high "mobility" during deposition.
fill evrywhere including recesses and holes it "see' during
Remember the cross section of the MUMP process that Cronos
Web page for illustration purpose. The structural poly even
recess under a roof structure. It basically coats everywher
the reacting gas.
I will suggest that standard MEMS provided a SEM picture of
after poly deposition so we will have a better understanding
problem was.
They may want to dip the wafer in buffered HF for 30 second
the wafer so we can see layer structures.
It will be helpful if they can provide the deposition recipe
polysilicon deposition. We can compare their recipe with
Michigan or Cornell. This may provide some clues to the

Regards,
Jingkuang Chen

CC: Tom Pumo <TPumo@smems.com>, Glenn Fricano <GFrican...

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: "Bruce Scharf" <Opto-man@microscan.com>
Date: Thu, Apr 19, 2001 1:12 PM
Subject: RE: FW: Optical MEMS Manufacturing Consortium

Will do. This would be a pretty ugly change, both in terms of capital equipment and intellectual property, but having an alternative supplier is the only way I can think of to put pressure on Standard MEMS to deliver!

Regards,

Joel

-----Original Message-----

From: Bruce Scharf [mailto:Opto-man@microscan.com]
Sent: Thursday, April 19, 2001 1:15 PM
To: JKubby@crt.xerox.com
Subject: Re: FW: Optical MEMS Manufacturing Consortium

Consortium

Thanks for the update Joel. If they would like to speak with another partner in the consortium, please feel free to give them my contact info.

Bruce

>>> "Kubby, Joel A" <JKubby@crt.xerox.com> 04/19 8:17 AM >>>
Bruce,

FYI. I am looking into ADI as a possible alternate supplier. Please keep this quiet. I am just trying to find out what our options are (if any). Once we determine what our options are we can then consider if we want to set deadlines with Standard MEMS.

Regards,

Joel

-----Original Message-----

From: Kubby, Joel A
Sent: Thursday, April 19, 2001 11:13 AM
To: 'Zawadzki, Dave'
Cc: 'G. V. Blessing'; Kubby, Joel A
Subject: Optical MEMS Manufacturing Consortium

<<Paper OE 4293-07.pdf>>

Dave,

I hope all is going well for you at Analog. I was wondering if you could see if there would be any interest on the part of ADI to get involved with a MOEMS Manufacturing Advanced Technology Program administered

*U.S. Patent Application Serial No. 10/000,232
Declaration of Bruce R. Scharf and Troy Daiber
Exhibit B13 (page 1 of 2)*

by NIST. I have attached a recent publication describing the work that is being done in this project. One of our partners is having a hard time meeting our delivery schedule and we want to investigate alternate suppliers. I know that ADI recently bought BCO Technologies, a leading supplier of SOI wafers, so I thought this project might be of strategic interest for their optical MEMS program. Could you forward this note on to the appropriate persons in the optical MEMS area to see if there would be any interest?

At this point we are only seeking to find out what our alternatives are.

Thanks for any help you can provide.

Best Regards,

Joel

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: "Bruce Scharf" <Opto-man@microscan.com>
Date: Tue, Jul 17, 2001 7:53 AM
Subject: RE: Proposed agenda for 3Q01ATP R&D Coordination Meeting

Bruce,

Yes, I was thinking along the same lines. Probably do a critical point release and assembly. We can coordinate this at the meeting.

Regards,

Joel

—Original Message—

From: Bruce Scharf [mailto:Opto-man@microscan.com]
Sent: Tuesday, July 17, 2001 10:40 AM
To: JKubby@crt.xerox.com
Subject: Re: Proposed agenda for 3Q01ATP R&D

Coordination Meeting

Joel,

I'll be there. As we plan the Mask Set 1 testing, it may make sense to have Andy join you guys in Rochester for a week....what do you think?

Bruce

Bruce R. Scharf
Engineering Director
Microscan Systems, Inc.

>>> "Kubby, Joel A" <JKubby@crt.xerox.com> 07/16 2:44 PM >>>
<<3Q01 R&D Coordination Meeting Agenda.doc>> <<Directions
to SMSC.doc>>

All,

Please find attached a proposed agenda for our upcoming 3Q01
R&D

Coordination meeting, to be held on Thursday and Friday,
August 2nd & 3rd at
Standard MEMS in Hauppauge NY. I have also attached driving
instructions
and the suggest hotel. Please RSVP so I can get a count of
the number of
people that will be attending. I will be looking forward to
seeing you in
Hauppauge in a couple of weeks!

Regards,

Joel

MOEMS Manufacturing Consortium '01 Schedule (revised 8/3/01)

	<i>Start</i>	<i>End</i>
1. Mask Set I (SMEMS)	6/06/00	9/30/01
2. Fab CMOS/DMOS (Xerox)	1/15/01	4/30/01
3. Test CMOS/DMOS (Xerox)	4/30/01	7/30/01
4. Revise CMOS/DMOS (Xerox)	7/30/01	9/15/01
5. Mask Set I Post-Process (Xerox)	9/30/01	10/01/01
6. Mask Set I Package (Xerox)	10/01/01	11/01/01
7. Mask Set I Test (Microscan, Xerox)	10/01/01	10/15/01
8. Fab CMOS/DMOS (SMEMS)	3/01/01	10/03/01
9. Mask Set II Layouts (All)	10/15/01	11/01/01
10. Mask Set II Layout Freeze	11/01/01	
11. Mask Set II Fabrication	11/01/01	9/06/02

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: "Bruce Scharf" <Opto-man@microscan.com>
Date: Sun, Aug 12, 2001 9:36 AM
Subject: RE: atp back side gold

Thanks for the feedback Bruce. I think our applications should be OK with only frontside metallization so long the backside metallization is not required for stress balancing of the frontside metallization or for eutectic die attach. I will check on the eutectic die attach.

Regards,

Joel

-----Original Message-----

From: Bruce Scharf [mailto:Opto-man@microscan.com]
Sent: Friday, August 10, 2001 7:11 PM
To: JKubby@crt.xerox.com
Subject: RE: atp back side gold

Joel,
In case Andy didn't respond yet, no we do not use the
backside gold.
Bruce

<<< "Kubby, Joel A" <JKubby@crt.xerox.com> 8/10 8:55a >>>
All,

If anyone required backside gold for their designs, could
you let me know?

Thanks,

Joel

-----Original Message-----

From: Dave Kharas
[mailto:DKharas@smems.com]
Sent: Thursday, August 09, 2001 12:48 PM
To: 'Kubby, Joel A'
Subject: atp back side gold

Hi Joel,
we had another question on the ATP process
flow.

There was an optional step after the KOH
etching for back
side gold,

do any of the partners need gold on the back
side?
if so we will need to do the following steps
after KOH etch:

- 1: Gello strip
- 2: Tegal back side nitride etch

3: Coat with photo resist 3 mic front side
 4: wet etch 8:1 BOE 4 min.
 5: strip PR
 6: back side gold evaporation 1000A
 7: coat front side protective PR and ship

Also Nimal need JK to send him the optimized

DMOS conditions
 that he wants

us to run
 thanks

dave

—Original Message—

From: Kubby, Joel A

[mailto:JKubby@crt.xerox.com]

Sent: Wednesday, August 08, 2001 2:12 PM

To: 'Dave Kharas'

Subject: RE: Minutes and actions items from

ATP 3Q01 R&D

Coordination

meet ing, August 2nd & 3rd @ Standard MEMS

138 TEOS anchor

etch should

the group to

make sure that

Thanks Dave. I think we wrote down that the

stop on SCS, but I will send the note out to

everyone is aware.

Regards,

Joel

—Original Message—

From: Dave Kharas

[mailto:DKharas@smems.com]

Sent: Wednesday, August

08, 2001 2:01 PM

To: 'Kubby, Joel A'

Subject: RE: Minutes

and actions

items from ATP 3Q01

R&D Coordination meet ing, August 2nd & 3rd

@ Standard MEMS

rule addendum.

i thought of another design

the teos anchor at 138

should stop on SCS

and not on any

opening created

in the scs etches 130,132,

136. Thus it

would fix the etch
depth at 2
microns,
rather than a variable
depth.

regards
dave

-----Original Message-----
From: Kubby, Joel A
[mailto:JKubby@crt.xerox.com]
Sent: Wednesday, August 08,
2001 1:32 PM
To: 'Nimal De Lanerolle'
Cc: aseck@smems.com; Chris
Nichols;
dkharas@smems.com; Glenn
Fricano;
jobrien@smems.com; Nena
Liakopoulos; Steve
Delvecchio; Tom
Pumo
Subject: RE: Minutes and
actions items from
ATP 3Q01 R&D
Coordination
meet ing, August 2nd & 3rd @
Standard MEMS

Nimal,
Have each person who would
like to be
registered send me an
e-mail note with
the user name and password
they would like
to have and I
will set them up
with an account.

Thanks,
Joel

-----Original Message-----

Nimal De Lanerolle

[mailto:NDeLanerolle@smems.com]

Wednesday, August
08, 2001 1:03 PM

From:

Sent:

To:

*U.S. Patent Application Serial No. 10/000,232
Declaration of Bruce R. Scharf and Troy Daiber
Exhibit B16 (page 3 of 4)*

'joel.kubby@crt.xerox.com'

FW: Minutes
and actions
items from ATP 3Q01
R&D Coordination meeting,
August 2nd & 3rd
@ Standard MEMS

maskset1_v8.xst >>
Joel

in the present
team have access
to the ATP web
site. Could you
provide us
with the password
etc. Thanks.

Subject:

<< File:

None of us

Nimal

-----Original Message-----

Gulvin, Peter
[mailto:PGulvin@crt.xerox.com]

Monday, August 06,
2001 12:50 PM

Joel A;
'art@memcad.com';
'aseck@smems.com';
'azosel@microscan.com';
Chua, Christopher
<chua@parc.xerox.com>;
'cnichols@smems.com';
DeBruyker, Dirk
<ddebruyk@parc.xerox.com>;
'dkharas@smems.com';
'd

From:

Sent:

To: Kubby,

From: Andy zosel
To: "JKubby@crt.xerox.com"@Microscan.GWIA
Date: Fri, Sep 7, 2001 1:11 PM
Subject: Re: FW: HF release and etch rates from ATP wafer # 1.

Joel,

I have attached a memo summarizing our initial release experience.

Andy

>>> "Kubby, Joel A" <JKubby@crt.xerox.com> 08/23 9:35 AM >>>
All,

Please find attached some initial release results for the lead lot Mask Set I parts. The data is preliminary, but it looks like a reasonable etch rate for the BOX is about 1 mm. The parts released in the attached file took somewhere between 10 and 20 minutes to release. At the 20 minute mark many of the parts were totally released from the chip (i.e. no longer attached). More data for intermediate etch times should be available soon. We will be shipping unreleased diced parts to the partners as soon as we receive some shipping containers, most likely some time next week.

Regards,

Joel

-----Original Message-----

From: Diehl, James C
Sent: Wednesday, August 22, 2001 11:12 AM
To: Harvey, Chris; Tshudy, Dwight J; Feng, James; Larussa, Joe; Kubby, Joel A; Meyers, John P; Feinberg, Kathleen; Herko, Lawrence H; Gulvin, Peter; Nystrom, Peter; Jia, Nancy; Kennedy, William L; Folger, William F; German, Kristine
Subject: HF release and etch rates from ATP wafer # 1.

Please find in the attached file, a report documenting the HF release and etch rates from ATP wafer # 1. This is mainly a collection of pictures taken by Larry and myself before and after HF release as well as 10 & 20 Min comparisons.

<<ATP WAFER 1 before - after comparisons 10 & 20 Min HF.doc>>

CC: Bruce Scharf; Bryan Davis; Malinda Elie

From: "Kubby, Joel A" <JKubby@crt.xerox.com>
To: "Kubby, Joel A" <JKubby@crt.xerox.com>, "art@memc...
Date: Fri, Sep 28, 2001 12:40 PM
Subject: RE: ATP Teleconference Call on Monday, October 1st to discuss Mask Set 1 test results

All,

We do not have any further test results beyond the problems we have already identified, so it does not look like a teleconference call would be beneficial on Monday, October 1st. Standard MEMS outlooks delivery of the follow-on wafers that have the correct TEOS thickness, and better anchored parts, by October 15th. It will take us about two weeks to dice, release and test the parts before we have significant information, so it may be better to delay our 4Q00 meeting until the beginning of November. I would propose either Thursday & Friday November 1st and 2nd, or Monday and Tuesday, November 5th and 6th. If anyone planning on attending has a conflict for either of these dates, let me know. If there are no conflicts reported back in the next few days, I will send out the final date.

Best Regards,

Joel

—Original Message—

From: Kubby, Joel A
Sent: Thursday, September 13, 2001 5:46 PM
To: art@memcad.com; aseck@smems.com; azosel@microscan.com; Christopher Chua; cnichols@smems.com; Dirk DeBruyker; dkharas@smems.com; dzaharek@smems.com; Eric Peeters; fbriganti@smems.com; gblessing@nist.gov; gficano@smems.com; James Calamita; James Diehl; Jingkuang Chen; jobrien@smems.com; Joel Kubby; John Meyers; jrg@memcad.com; Lawrence Herko; Malinda Elien; Michel Rosa; Nancy Jia; ndelanerolle@smems.com; Nena Liakopoulos; ngolubovic@smems.com; opto-man@microscan.com; Peter Gulvin; Peter Nystrom; rkmal@prodigy.net; rvl@memcad.com; sbart@memcad.com; sdelvecchio@smems.com; szhou@smems.com; tedp@memcad.com; tom.korsmeyer@memcad.com; Tony Paine; tpumo@smems.com
Subject: ATP Teleconference Call on Monday, October 1st to discuss Mask Set 1 test results

All,

I hope everyone is OK after the terrorist attack earlier this week and that no one lost family or friends. Given the difficulties in arranging air travel following this event, it is probably best to stay with our original plans for our 4Q01 R&D Coordination meeting later in October. Hopefully by then air travel will be back as close as possible to normal. I would like to propose a teleconference call for the afternoon of Monday, October 1st from 1-3 PM (eastern) to review Mask Set 1 test results. I have posted the test results I have received so far on our website at:

http://206.236.85.4/forum/dri-1/_w/dispatch-w.cgi/_T_MEMS-ATP_docshare/showFolder/101182
<http://206.236.85.4/forum/dri-1/_w/dispatch-w.cgi/_T_MEMS-ATP_docshare/showFolder/101182>

*U.S. Patent Application Serial No. 10/000,232
Declaration of Bruce R. Scharf and Troy Daiber
Exhibit B18 (page 1 of 2)*

Hopefully by 10/1 we will have been able to test the follow-on lots of Mask Set 1 wafers that have backside release holes and improved TEOS quality (less cracking). I will post any additional test results received on the website at this location prior to the teleconference call so that they will be available during the meeting. Let me know if you have a conflict for this date and time.

Thanks,

Joel

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